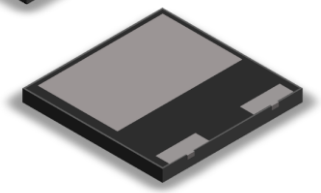


GPT65Z3YMR

650V ▲ 245mΩ ▲ GaN FET

GALLIUM NITRIDE GaN FET ▲ SMD type
Normally off device
Easy to drive with standard MOSFET driver
Ultra-thin DFN8080 package with 0.9mm height
Moisture Sensitivity Level ▲ MSL 3
Ultra-low Q_{RR} and very robust design

SPECIFICATION

Item (T_C = 25°C, unless otherwise noted)		Characteristics
Operating Temperature Range	T_J	-55°C to +150°C
Storage Temperature Range	T_S	-55°C to +150°C
Drain-Source Voltage	V_{DSS}	650V
Transient Drain-Source Voltage Note 1	$V_{TR(DSS)}$	800V
Drain-Source On-State Resistance Note 2	$R_{DS(ON)TYP}$	245mΩ
Typical Recovered Charge Note 3	Q_{RR}	40nC
Typical Total Gate Charge	Q_G	22nC

Notes

1: **Spike duty cycle DC < 0.01, spike duration time < 20µs during off-state mode**

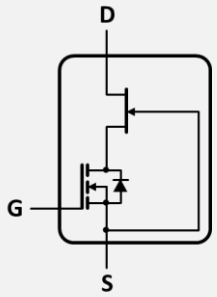
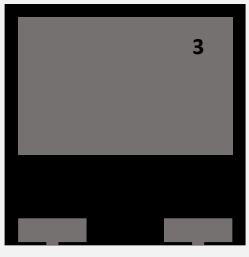
2: **V_{GS} = 8V, I_D = 4A, T_J = 25°C**

3: **See diode reverse recovery test circuit and waveform, Fig. 17, and Fig. 18**

APPLICATIONS

Battery Chargers	Power Adapters	LED Lighting	Wireless Power	AC/DC Converter	DC/DC Converter	Class D Audio Amplifiers
						

PIN DESCRIPTION

Circuit Diagram	Outline ▪ Bottom View	Pin No.	Symbol	Description
		1 2 3	G D S	Gate Drain Source

STORAGE AND HANDLING CONDITIONS

ESD level	Floor life	Conditions	MSL
HBM class 2	168 hours	T_A < 30°C, RH < 60%	3

ABSOLUT MAXIMUM RATINGS ▲ T_C = 25°C, unless otherwise noted

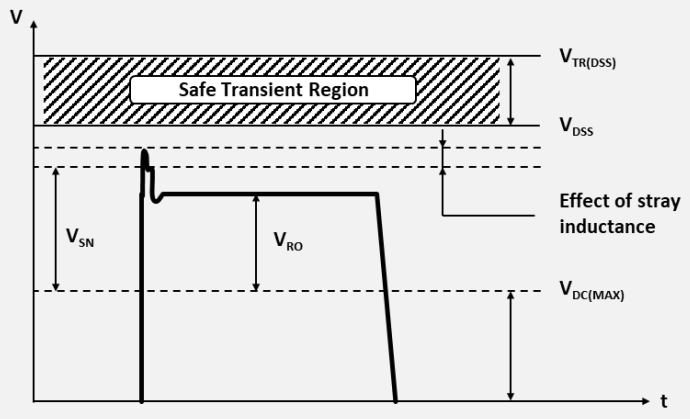
Item	Condition	Symbol	Limit	Unit
Drain-Source Breakdown Voltage		V_{DSS}	650	V
Transient Drain-Source Voltage Note1		$V_{(TR)DSS}$	800	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	T_C = 25°C Note 2	I_D	9	A
Continuous Drain Current	T_C = 100°C Note 2	I_D	6	A
Pulse Drain Current	T_C = 25°C, Pulse Width = 10µs	I_{DM}	31	A
Maximum Power Dissipation	T_C = 25°C	P_D	38	W
Operating Temperature Range	Case	T_C	-55 to +150	°C
Operating Temperature Range	Junction	T_J	-55 to +150	°C
Storage Temperature Range		T_S	-55 to +150	°C

Note:

1: Spike duty cycle DC < 0.01, spike duration time < 20µs during off-state mode

2: See application information for increased stability at high current operation, fig. 2

Fig. 1 ▪ Voltage Stress Primary Switch with 264VAC



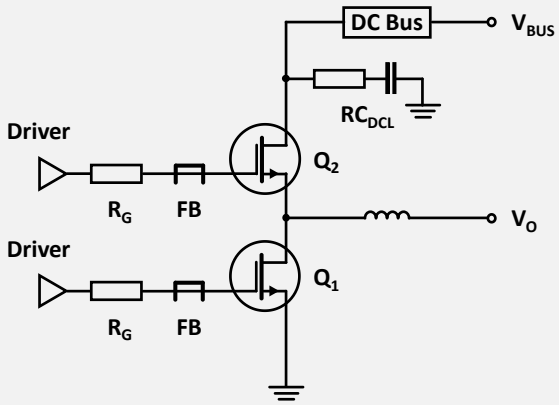
$V_{TR(DSS)}$ - V_{DSS} = Safety margin
800V - 650V = 150V
Safety margin is around 80%

$V_{DC(MAX)}$ + V_{SN} + effect of stray inductance < 560V

$V_{DC(MAX)}$	Maximum input voltage
V_{RO}	Reflected output voltage
V_{SN}	Snubber capacitor voltage
V_{DSS}	Drain-Source breakdown voltage
$V_{(TR)DSS}$	Transient Drain-source voltage

APPLICATION INFORMATION

Fig. 2 ▪ Recommended Circuit for Improved Stability at High Current Operation



A ferrite bead (FB) should be connected in series with the gate pin to dampen the resonant circuit of gate-source loop inductance and the input capacitance of the GaN-FET. The ferrite bead should be placed as close as possible to the gate pin to minimize the gate-source loop. (See figure 2). This causes fast switching stability. We recommend an impedance of 470Ω at 100MHz for the ferrite bead. In addition, a series resistance (R_G) of 33Ω should be provided.

Furthermore, a DC-link snubber should always be used to eliminate instability of the GaN-FET. In the simplest case, an RC combination is connected in parallel to the DC link bus, which significantly reduces the Q factor of any resonance in the bus. We recommend an MLCC with 68pF and an SMD resistor with 15Ω as well-suited values.

THERMAL CHARACTERISTIC RATINGS

Items		Typ.
Thermal Resistance Junction to Ambient Note 1	R_{thJA}	50°C/W
Thermal Resistance Junction to Case	R_{thJC}	3.3°C/W

Note:

1: Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm² copper and 70µm thickness

ELECTRICAL CHARACTERISTICS ▲ T_C = 25°C, unless otherwise noted

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	V_{GS} = 0V	V_{DSS}	650			V
Gate-Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 500μA	V_{GSth}	1	1.6	2.5	V
Gate-Source Leakage Current	V_{GS} = 20V, V_{DS} = 0V	I_{GSS}			150	nA
Gate-Source Leakage Current	V_{GS} = -20V, V_{DS} = 0V	I_{GSS}			-150	nA
Drain-Source Leakage Current	V_{DS} = 650V, V_{GS} = 0V	I_{DSS}		10	20	μA
Drain-Source Leakage Current	V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C	I_{DSS}		50		μA
Drain-Source On-State Resistance	V_{GS} = 8V, I_D = 4A	$R_{DS(ON)}$		245	300	mΩ
Drain-Source On-State Resistance	V_{GS} = 8V, I_D = 4A, T_J = 150°C	$R_{DS(ON)}$		500		mΩ

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Dynamic Characteristics						
Input Capacitance	V_{DS} = 650V, V_{GS} = 0V, f = 1MHz	C_{ISS}		500		pF
Output Capacitance	V_{DS} = 650V, V_{GS} = 0V, f = 1MHz	C_{OSS}		20		pF
Reverse Transfer Capacitance	V_{DS} = 650V, V_{GS} = 0V, f = 1MHz	C_{RSS}		2		pF
Effective Output Capacitance, Energy Related Note 1	V_{DS} = 0 to 650V, V_{GS} = 0V	$C_{O(ER)}$		25		pF
Effective Output Capacitance, Time Related Note 2	V_{DS} = 0 to 650V, V_{GS} = 0V	$C_{O(TR)}$		45		pF
Total Gate Charge	V_{DS} = 400V, V_{GS} = 0 to 12V, I_D = 5.5A	Q_G		22		nC
Gate-Source Charge	V_{DS} = 400V, V_{GS} = 0 to 12V, I_D = 5.5A	Q_{GS}		3		nC
Gate-Drain Charge	V_{DS} = 400V, V_{GS} = 0 to 12V, I_D = 5.5A	Q_{GD}		3.5		nC
Output Charge	V_{DS} = 0 to 650V, V_{GS} = 0V	Q_{OSS}		32		nC
Turn-On Delay	V_{DS} = 400V, V_{GS} = 0 to 12V, I_D = 3A, R_G = 30Ω	$t_{D(ON)}$		20		ns
Rise Time	V_{DS} = 400V, V_{GS} = 0 to 12V, I_D = 3A, R_G = 30Ω	t_R		7		ns
Turn-Off Delay	V_{DS} = 400V, V_{GS} = 0 to 12V, I_D = 3A, R_G = 30Ω	$t_{D(OFF)}$		80		ns
Fall Time	V_{DS} = 400V, V_{GS} = 0 to 12V, I_D = 3A, R_G = 30Ω	t_F		6		ns

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Source-Drain Diode						
Source-Drain Voltage	I_S = 2A, V_{GS} = 0V	V_{SD}		1		V
	I_S = 5A, V_{GS} = 0V			1.5		V
Reverse Recovery Time Note 3	I_S = 3A, V_{GS} = 0V, V_{DS} = 400V, di/dt = 1000A/μs	t_{RR}		12		ns
Recovered Charge Note 4	I_S = 3A, V_{GS} = 0V, V_{DS} = 400V, di/dt = 1000A/μs	Q_{RR}		40		nC

Notes:

1: Equivalent capacitance to give same stored energy from 0V to the stated V_{DS}
2: Equivalent capacitance to give same charging time from 0V to the stated V_{DS}
3: See diode reverse recovery test circuit and waveform, fig. 17 and fig 18
4: See diode reverse recovery test circuit and waveform, fig 17 and fig. 18

REFERENCE DATA

Fig. 3 ▪ Typ. Output Characteristics I_D vs. V_{DS}, T_J = 25°C

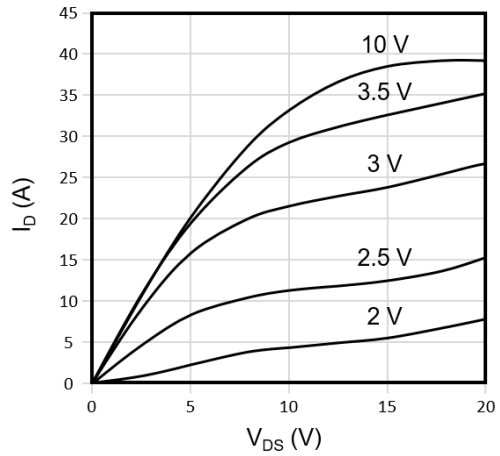


Fig. 4 ▪ Typ. Output Characteristics I_D vs. V_{DS}, T_J = 150°C

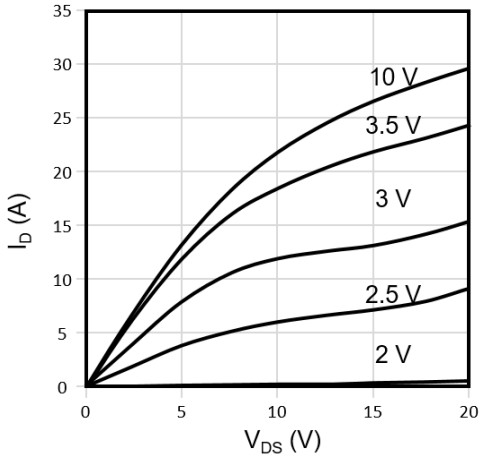


Fig. 5 ▪ Typ. Transfer Characteristics I_D vs. V_G, V_{DS} = 10V

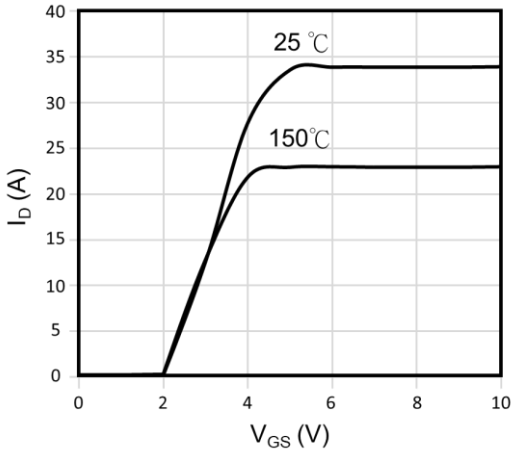


Fig. 6 ▪ Normalized $R_{DS(ON)}$ Characteristics, I_D = 4A, V_{GS} = 8V

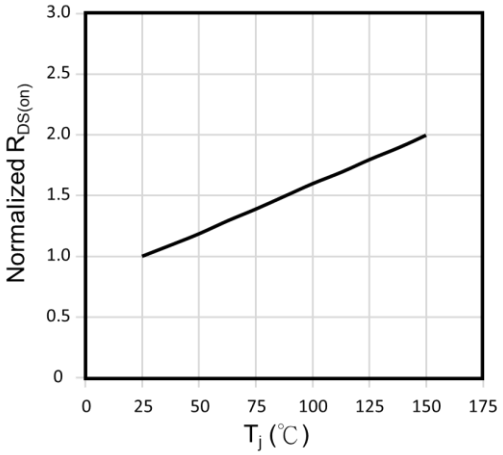


Fig. 7 ▪ Typ. Capacitance Characteristics, V_{GS} = 0V, f = 1MHz

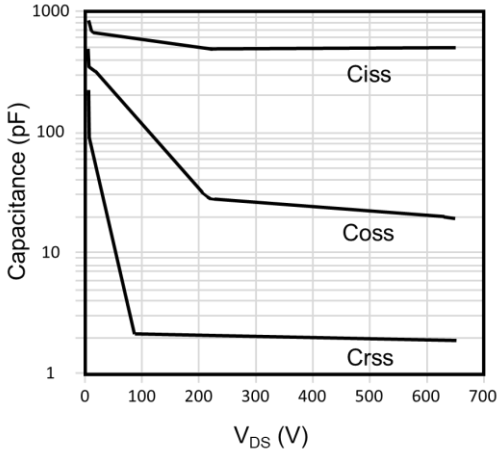
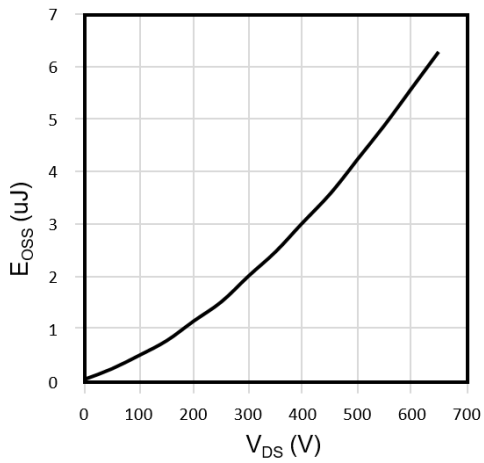


Fig. 8 ▪ Typ. Stored Energy Characteristics C_{OSS}



REFERENCE DATA

Fig. 9 ▪ Typ. Output Charge Q_{OSS} vs. Drain Voltage V_D

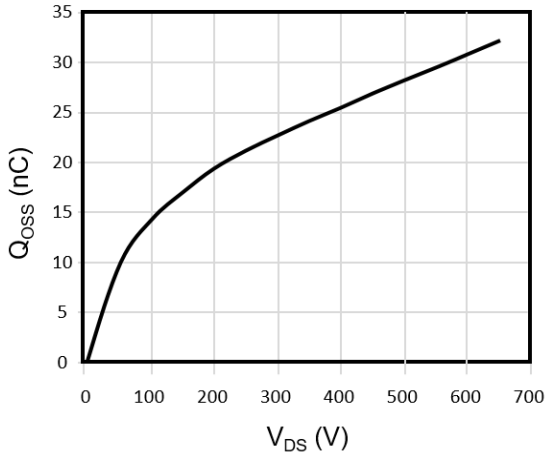


Fig. 10 ▪ Forward Characteristics of Reverse Diode $I_S = f(V_{SD})$

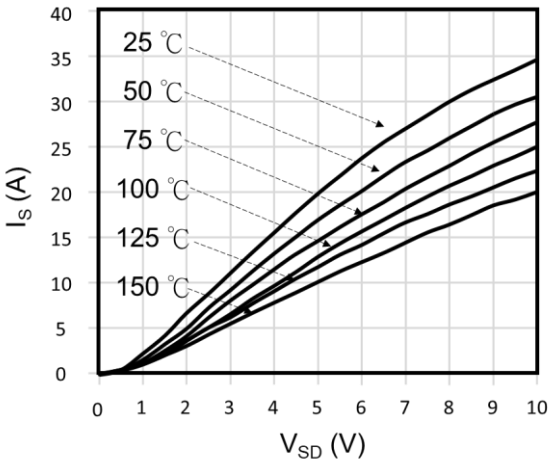


Fig. 11 ▪ Typ. Gate Charge Characteristics, I_D = 5.5A, V_{DS} = 400V

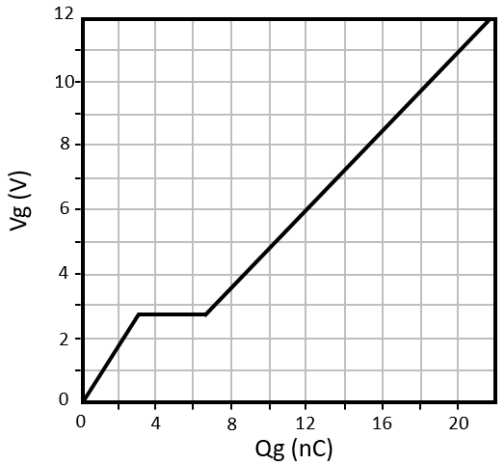


Fig. 12 ▪ Power Dissipation vs. Case Temperature T_C

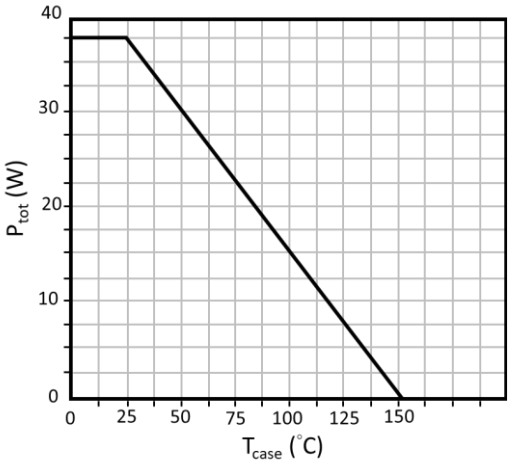


Fig. 13 ▪ Drain-Source Breakdown Voltage

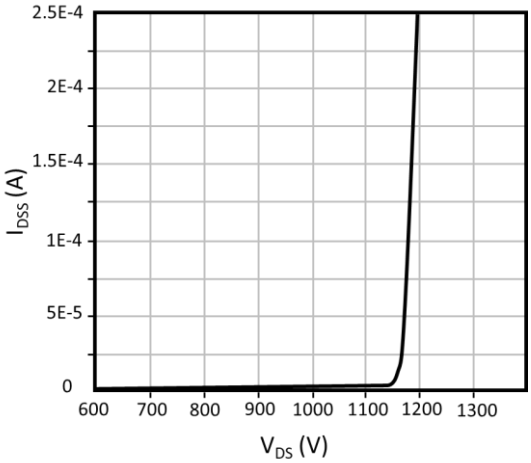
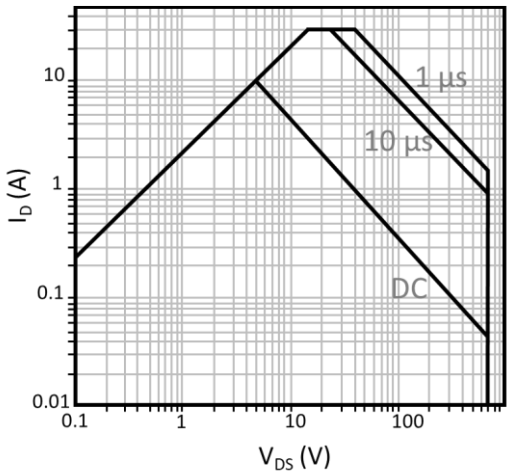


Fig. 14 ▪ Safe Operating Area, T_C = 25°C (calculated based on thermal limit)



REFERENCE DATA

Fig. 15 ▪ Safe Operating Area,
T_C = 80°C (calculated based on thermal limit)

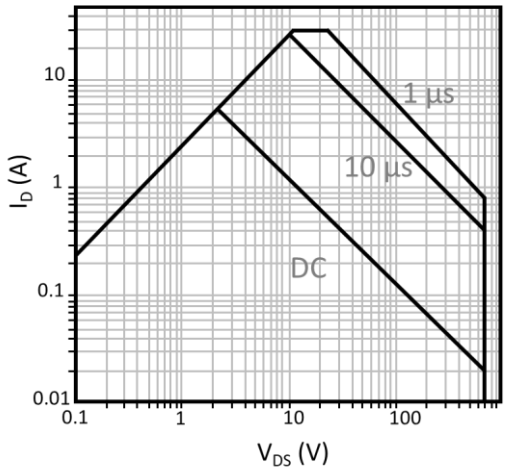
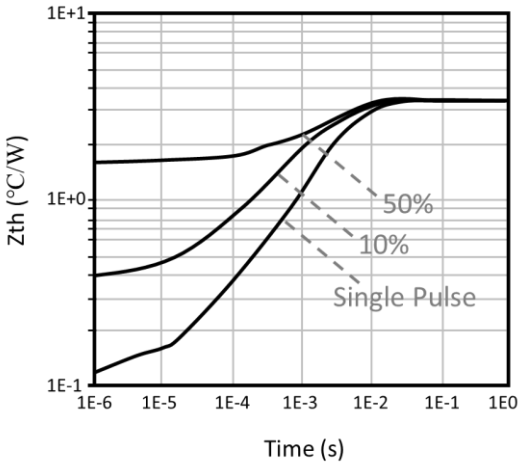


Fig. 16 ▪ Transient Thermal Impedance
Z_{thJC}



TEST CIRCUITS AND WAVEFORMS

Fig. 17 ▪ Diode reverse recovery test circuit

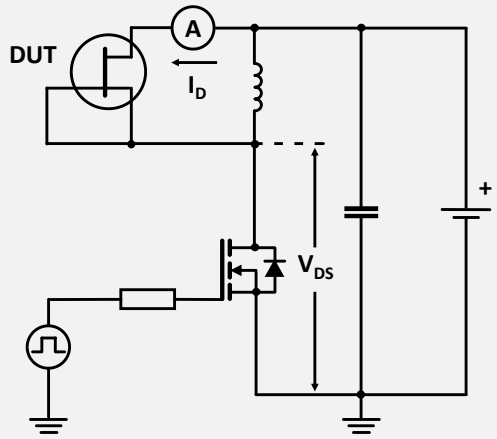


Fig. 18 ▪ Diode reverse recovery waveform

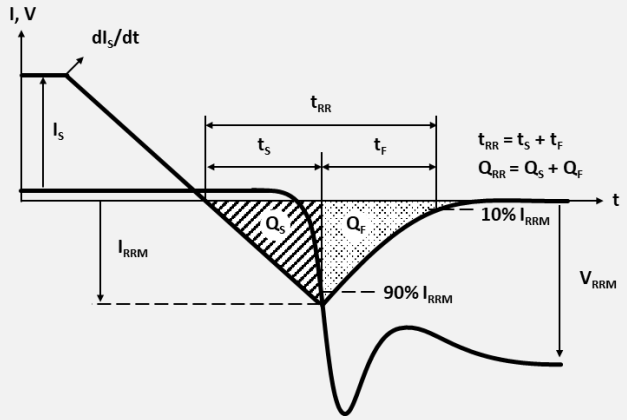


Fig. 19 ▪ Switching time test circuit

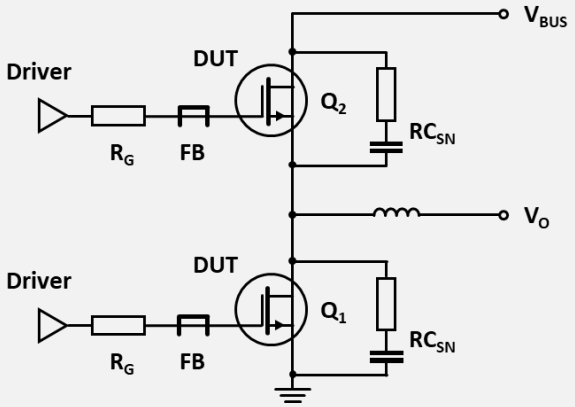


Fig. 20 ▪ Switching time waveform

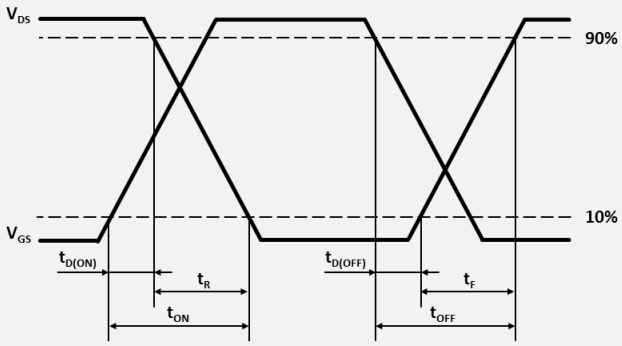


Fig. 21 ▪ Dynamic $R_{DS(ON)eff}$ test circuit

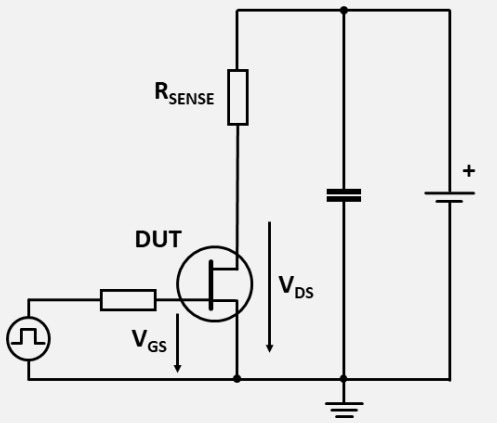
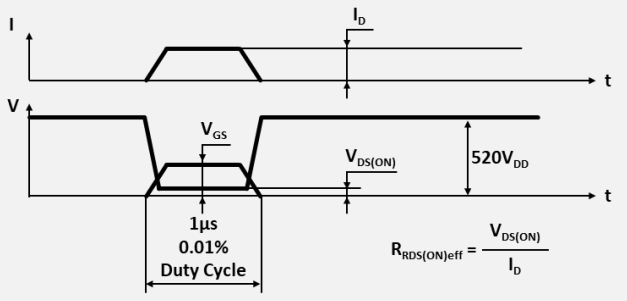


Fig. 22 ▪ Dynamic $R_{DS(ON)eff}$ waveform



LAYOUT GUIDELINES

The layout of GaN FETs is very important for performance and EMI due to the GaN FETs are normally operated under high voltage and high current. Figure 24 and Figure 25 show an example of a good power layout loop:

Fig. 23 ▪ Typical application schematic

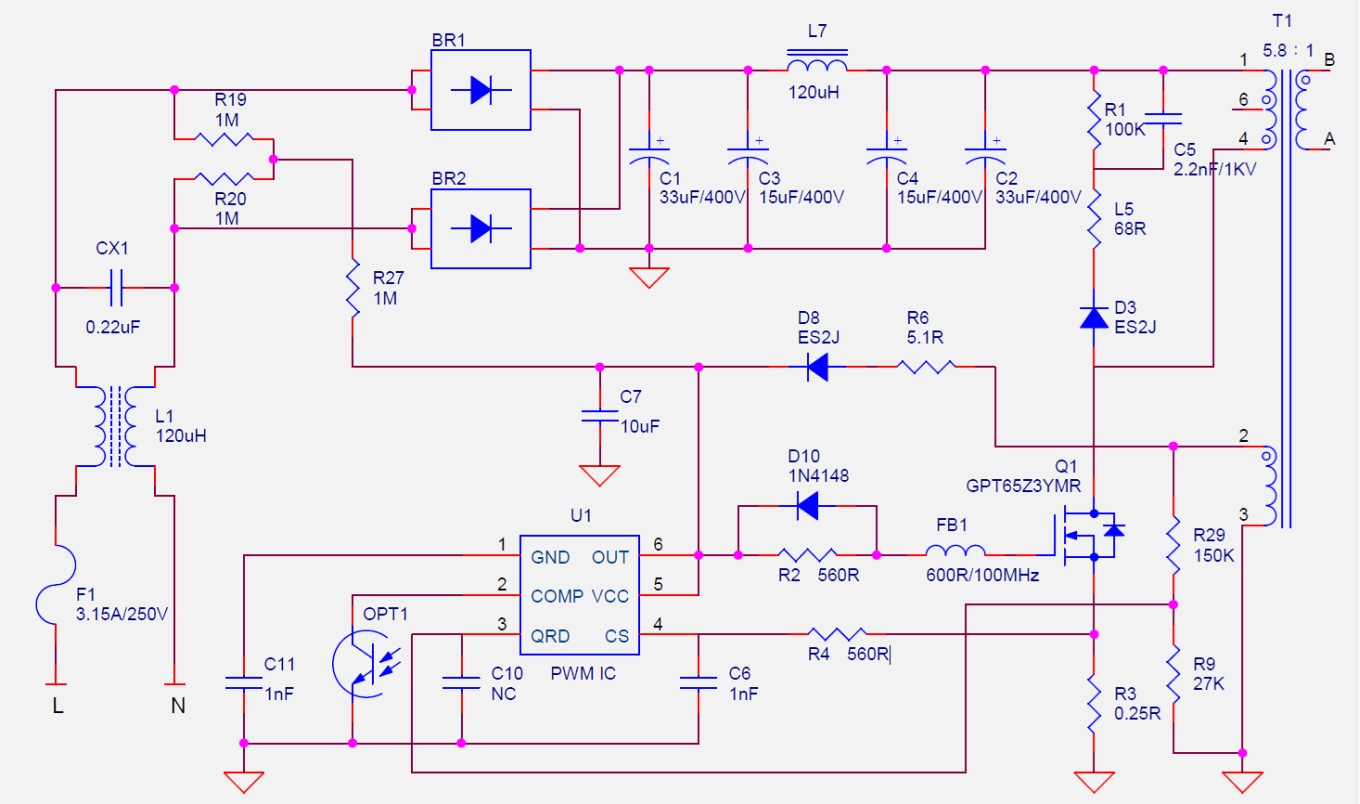


Fig. 24 ▪ Top layer for FR4 1.6mm

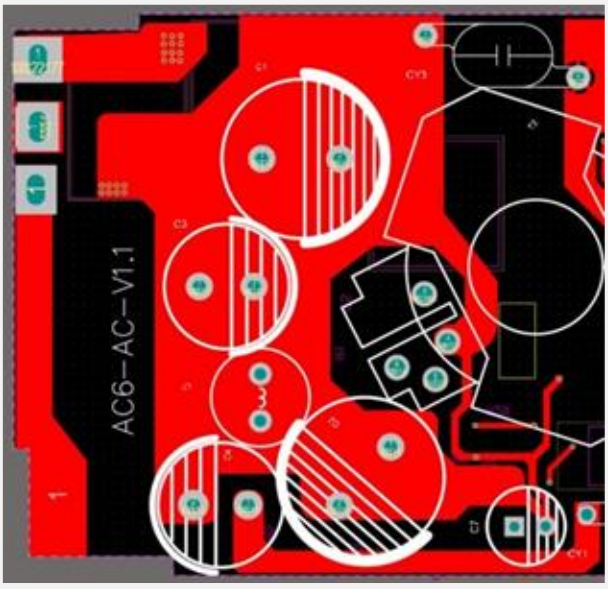
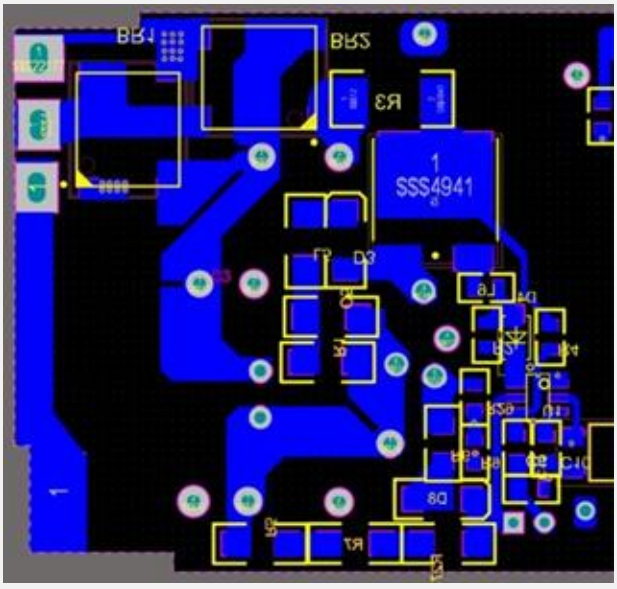


Fig. 25 ▪ Bottom layer for FR4 1.6mm



POWER-LOOP INDUCTANCE

The GaN FET has operated at a high transient current (di/dt) state. Therefore, the ringing, EMI, and voltage stress on GaN FET could be reduced by minimizing the inductance of the loop.

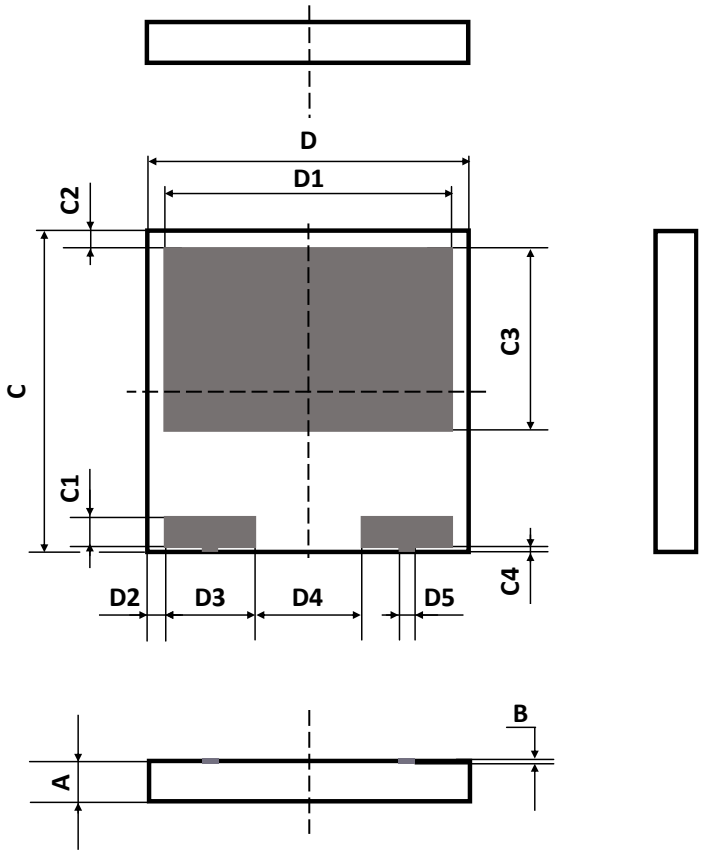
1. GND with a large area copper plane provides a low inductance ground for the GaN FET (Q1).
2. The power device GaN FET (Q1), diode (D3), and transformer (T1) are placed as close as possible to reduce the inductance.
3. The power device GaN FET (Q1) and resistor (R3) are placed as close as possible to reduce inductance and avoid abnormal switching.
4. Resistor (R3) and decoupling capacitor (C1) are placed as close as possible to minimize the current path and reduce the inductance.

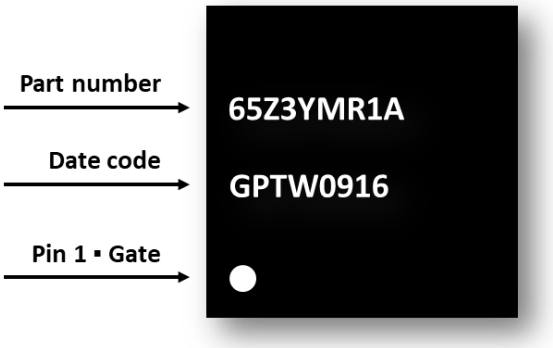
SWITCHING NODE CAPACITANCE

GaN devices have very low switching losses due to its low output capacitance and fast switching with high transient voltage (dv/dt). Therefore, additional capacitance on the output node should be minimized.

1. Shrinking the area of copper reduces the extra capacitance of the switching node.
2. Switching Node Trace should not overlap with Power plane and GND plane.
3. The copper plane of the Switching Node is not used for heat dissipation of the circuit board.

PACKAGE OUTLINE AND PART MARKING





Date code:
09: **e.g., week 09**
16: **e.g., 2022**

Sym	Millimeters
A	0.900 ± 0.050
B	0.203 ± 0.008
C	8.000 ± 0.050
C1	0.800 ± 0.025
C2	0.400 ± 0.025
C3	4.600 ± 0.050
C4	0.100 ± 0.025

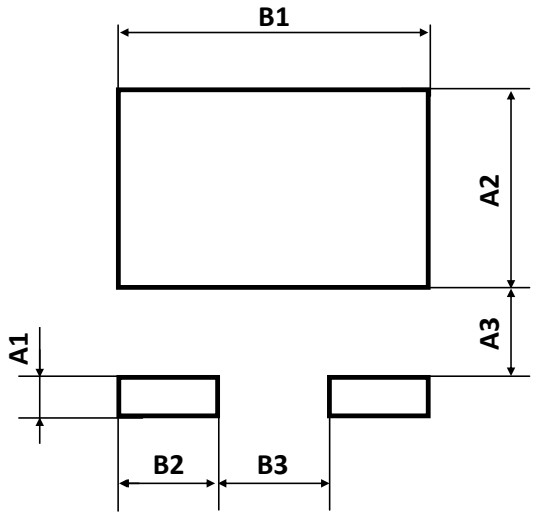
Sym	Millimeters
D	8.000 ± 0.050
D1	7.200 ± 0.050
D2	0.400 ± 0.025
D3	2.300 ± 0.025
D4	2.600 ± 0.025
D5	0.400 ± 0.025

DATE CODE

Example: **0916**

09		16	
Week of the Month		Year	
		16	2022
01	1st	17	2023
02	2nd	18	2024
03	3rd	19	2025
04	4th	1A	2026
...	...	1B	2026
52	52nd	...	...
		1F	2031

RECOMMENDED PAD LAYOUT FOR DFN 8080



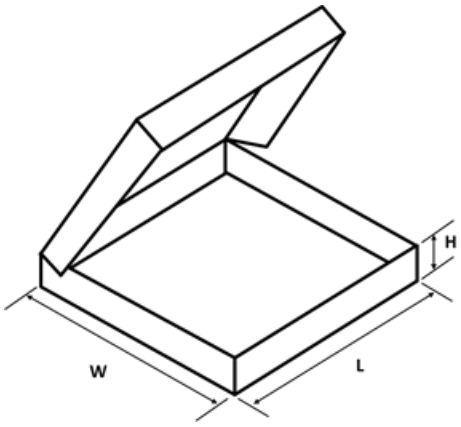
Sym	Millimeters
A1	1.000
A2	4.750
A3	2.000
B1	7.350
B2	2.450
B3	2.450

ORDERING INFORMATION

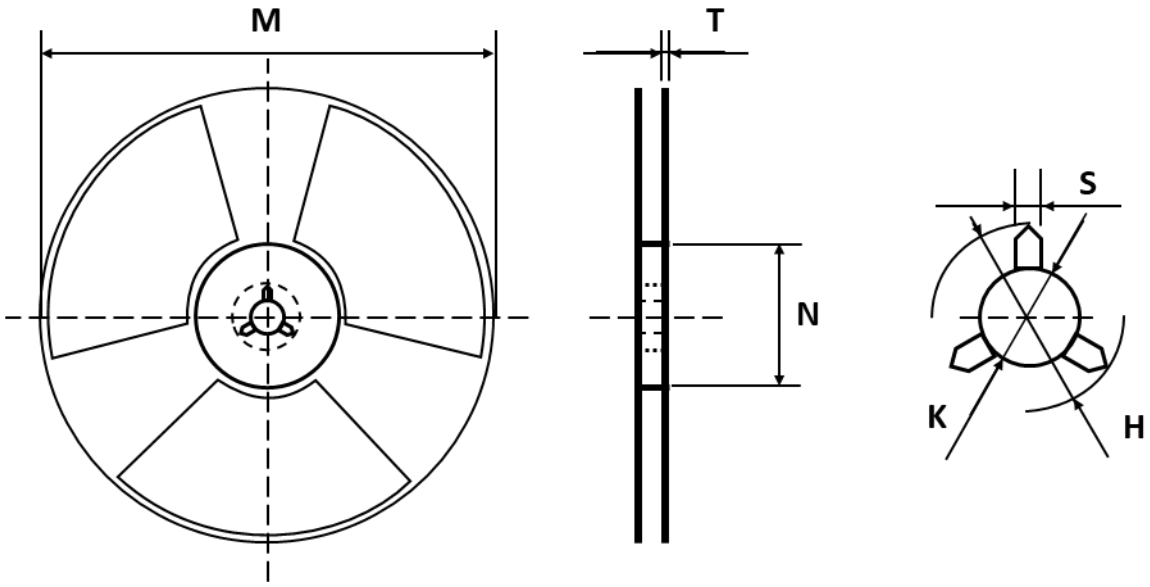
Part Number	Package	Packing	Quantity	Reel Diameter
GPT65Z3YMR	Thin DFN8080	Tape and Reel	2500pcs	330mm (13“)

REEL BOX DIMENSION ▲ All dimensions in mm

Outside Dimensions	
Ø 330mm reel	
W	350
L	350
H	80

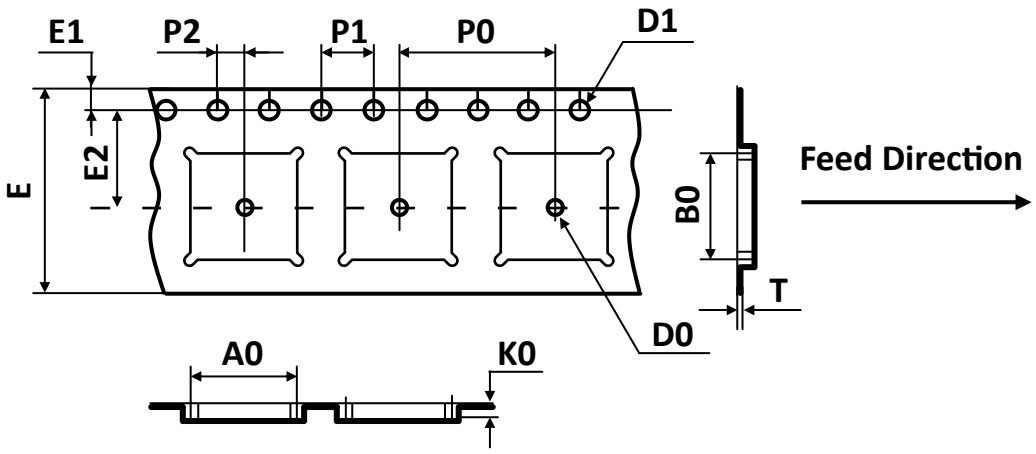


REEL DIMENSIONS ▲ All dimensions in mm



Tape Size	Reel Size	M	N	T	H	K	S
24mm	Ø330	Ø330.00	Ø102.00	2.00	13.00	10.50	2.00
		±0.20	±0.10	±2.0	+0.50 -0.20	±0.25	±0.25

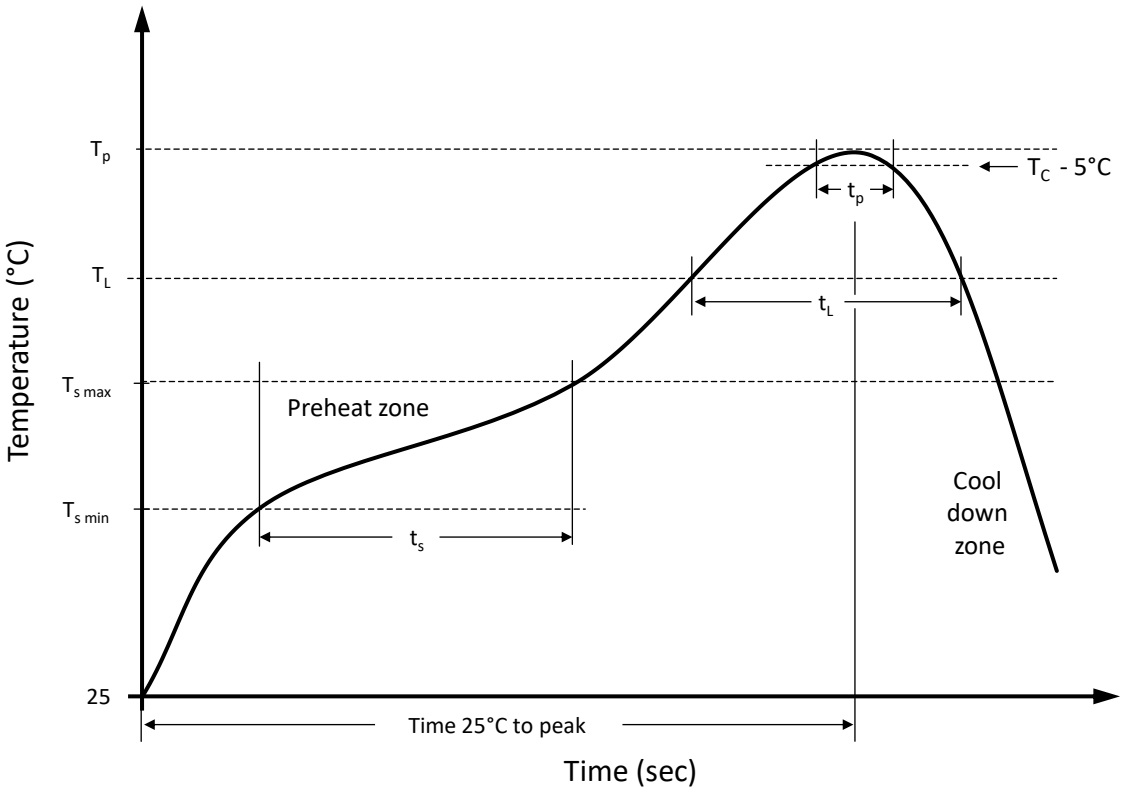
TAPE DIMENSIONS ▲ All dimensions in mm



Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN8080	8.30	8.30	1.15	1.50	1.50	24.00	1.75	7.50	12.00	4.00	2.00	0.30
	±0.10	±0.10	±0.10	±0.10	±0.10	±0.30	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05

Note: All dimensions meet EIA-481-D requirements.

RECOMMENDED REFLOW SOLDERING PROFILE



Recommended reflow soldering conditions ▲ Refer to JEDEC J-STD-020E

Profile Features		Sn-Pb Eutetic Assembly	Pb-Free Assembly
Preheat temperature min.	$T_{s\,min}$	100 °C	150 °C
Preheat temperature max.	$T_{s\,max}$	150 °C	200 °C
Preheat time t_s from $T_{s\,min}$ to $T_{s\,max}$	t_s	120 seconds	120 seconds
Ramp-up rate (T_L to T_p)		max. 3 °C/second	max. 3 °C/second
Liquidous temperature	T_L	183 °C	217 °C
Time t_L maintained above T_L	t_L	150 seconds max.	150 seconds max.
Peak package body temperature	T_p	235°C	260°C
Timeframe of within 5°C below and up to max actual peak body temperature	t_p	20 seconds max.	30 seconds max.
Ramp-down rate (T_L to T_p)		max. 6 °C/second	max. 6 °C/second
Time 25°C to peak temperature		max. 6 minutes	max. 8 minutes

REVISION TABLE

Revision	Date	Status	Notes
001	11/11/2022	Initial release	Initial publication

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